

Encounter manual

Guangyi CAO

Cadence Encounter is a software for placement and routing of synthesized vhdl (verilog) code.

To start with Encounter in linux, type **Encounter** in your home directory, then Encounter graphic user interface displays.

Create a folder, for example, **neededfile**, and put all needed files in it.

Necessary files should include:

1. A synthesized verilog file, like `fpu_sin.v`, or your own design.
2. Timing libraries, we use `typical_conditional_ccsm.lib`
3. lef file, `free2008_10_sp1.lef`
- 4 a clock tree file, `clock.ctsch`.

Import design

In encounter GUI, click design->import design, the following frame comes out, input all needed information like this. Please notice for top cell, you can choose Auto Assign.

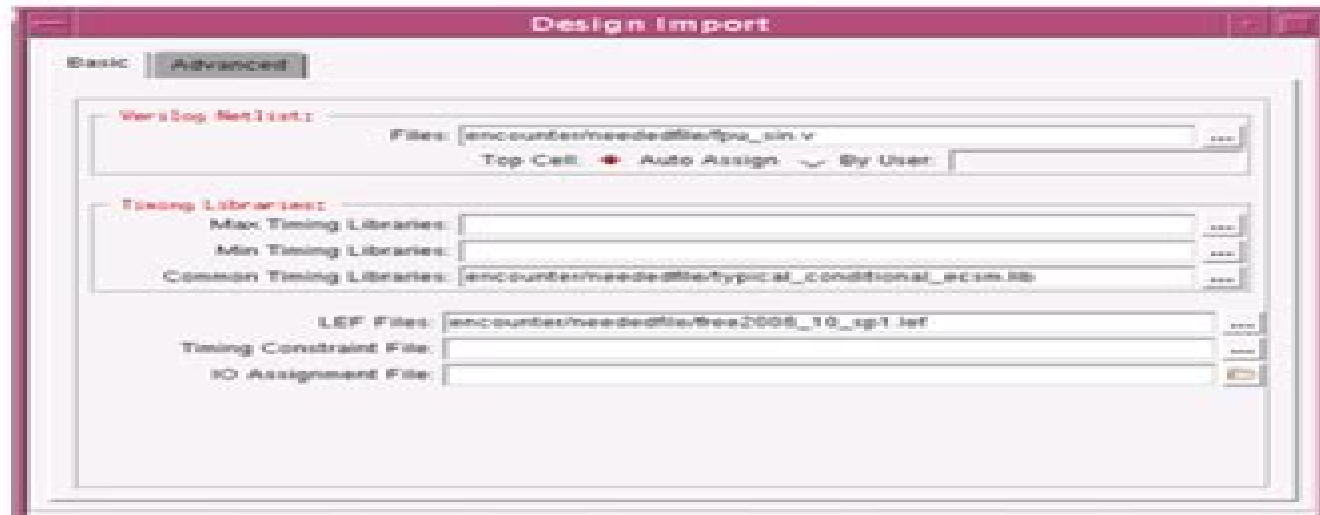


Figure 1

Cadence Encounter Timing User Manual

**Sandeep K. Goel, Krishnendu
Chakrabarty**



Cadence Encounter Timing User Manual:

Testing for Small-Delay Defects in Nanoscale CMOS Integrated Circuits Sandeep K. Goel, Krishnendu

Chakrabarty, 2017-12-19 Advances in design methods and process technologies have resulted in a continuous increase in the complexity of integrated circuits ICs. However, the increased complexity and nanometer size features of modern ICs make them susceptible to manufacturing defects as well as performance and quality issues. Testing for Small Delay Defects in Nanoscale CMOS Integrated Circuits covers common problems in areas such as process variations, power supply noise, crosstalk, resistive opens, bridges, and design for manufacturing DfM related rule violations. The book also addresses testing for small delay defects SDDs which can cause immediate timing failures on both critical and non-critical paths in the circuit. Overviews semiconductor industry test challenges and the need for SDD testing including basic concepts and introductory material. Describes algorithmic solutions incorporated in commercial tools from Mentor Graphics. Reviews SDD testing based on alternative methods that explore new metrics, top-off ATPG, and circuit topology based solutions. Highlights the advantages and disadvantages of a diverse set of metrics and identifies scope for improvement. Written from the triple viewpoint of university researchers, EDA tool developers, and chip designers and tool users, this book is the first of its kind to address all aspects of SDD testing from such a diverse perspective. The book is designed as a one-stop reference for current industrial practices, research challenges in the domain of SDD testing, and recent developments in SDD solutions. **Test**

and Diagnosis for Small-Delay Defects Mohammad Tehranipoor, Ke Peng, Krishnendu Chakrabarty, 2011-09-08 This book will introduce new techniques for detecting and diagnosing small delay defects in integrated circuits. Although this sort of timing defect is commonly found in integrated circuits manufactured with nanometer technology, this will be the first book to introduce effective and scalable methodologies for screening and diagnosing small delay defects including important parameters such as process variations, crosstalk, and power supply noise. Circuits and Systems Advances in Near

Threshold Computing Sanghamitra Roy, 2021-05-11 Modern society is witnessing a sea change in ubiquitous computing in which people have embraced computing systems as an indispensable part of day-to-day existence. Computation, storage, and communication abilities of smartphones, for example, have undergone monumental changes over the past decade. However, global emphasis on creating and sustaining green environments is leading to a rapid and ongoing proliferation of edge computing systems and applications. As a broad spectrum of healthcare, home, and transport applications shift to the edge of the network, near threshold computing (NTC) is emerging as one of the promising low-power computing platforms. An NTC device sets its supply voltage close to its threshold voltage, dramatically reducing the energy consumption. Despite showing substantial promise in terms of energy efficiency, NTC is yet to see widescale commercial adoption. This is because circuits and systems operating with NTC suffer from several problems, including increased sensitivity to process variation, reliability problems, performance degradation, and security vulnerabilities, to name a few. To realize its potential, we need designs

techniques and solutions to overcome these challenges associated with NTC circuits and systems The readers of this book will be able to familiarize themselves with recent advances in electronics systems focusing on near threshold computing

Energy-Efficient Communication Processors Robert Fasthuber, Francky Catthoor, Praveen Raghavan, Frederik Naessens, 2013-05-29 This book describes a new design approach for energy efficient Domain Specific Instruction set Processor DSIP architectures for the wireless baseband domain The innovative techniques presented enable co design of algorithms architectures and technology for efficient implementation of the most advanced technologies To demonstrate the feasibility of the author s design approach case studies are included for crucial functionality of advanced wireless systems with increased computational performance flexibility and reusability Designers using this approach will benefit from reduced development product costs and greater scalability to future process technology nodes *Nanometer Technology Designs* Nisar Ahmed, 2010-02-26 Adopting new fabrication technologies not only provides higher integration and enhances performance but also increases the types of manufacturing defects With design size in millions of gates and working frequency in GHz timing related defects havv become a high proportion of the total chip defects For nanometer technology designs the stuck at fault test alone cannot ensure a high quality level of chips At speed tests using the transition fault model has become a requirement in technologies below 180nm Traditional at speed test methods cannot guarantee high quality test results as they face many new challenges Supply noise including IR drop ground bounce and Ldi dt effects on chip performance high test pattern volume low fault defect coverage small delay defect test pattern generation high cost of test implementation and application and utilizing low cost testers are among these challenges This book discusses these challenges in detail and proposes new techniques and methodologies to improve the overall quality of the transition fault test

Design and Process Integration for Microelectronic Manufacturing ,2005 *FPGA ...* ,2006 *EDN* ,2005
Synthesis Methodology for Built-in At-speed Testing Yinghua Li, 2005 *A Low Power Design Methodology with Multi-VDD and Voltage Islands* Huaizhi Wu, 2007 *Electronic Business* ,2004 The management magazine for the electronics industry Voice & Data ,2005 **Integrated Circuit and System Design** ,2004 **Linguistics and Language Behavior Abstracts** ,2008 *Voice Enabling Web Applications* Ken Abbott, 2001-11-15 Developers can use the same technology to build both automated voice services as well as visual Web sites and Ken Abbott shows how in this comprehensive introduction to the syntax concepts and strategies relevant to VoiceXML **The Poet's Handbook** Judson Jerome, 1986 Detailed instruction in the mechanics and art of writing poetry *The American Organist* ,1993 **Orthotics and Prosthetics in Rehabilitation** Michelle M. Lusardi, Caroline C. Nielsen, 2007 Whether you are a student or a clinician if you work with patients with neuromuscular and musculoskeletal impairments you will find this text supplies a strong foundation in and appreciation for the field of orthotics and prosthetics that will give you the critical skills you need when working with this unique client population *Vogue* ,1953 **Music Teacher and Piano Student** ,1943

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