Encounter manual

Guangyi CAO

Cadence Encounter is a software for placement and routing of synthesized vhdl (verilog) code.

To start with Encounter in linux, type **Encounter** in your home directory, then Encounter graphic user interface displays.

Create a folder, for example, **neededfile**, and put all needed files in it.

Necessary files should include:

1. A synthesized verilog file, like fpu_sin.v, or your own design.
2. Timing libraries, we use typical_conditional_ecsm.lib
3. lef file, free2008_10_sp1.lef
4 a clock tree file, clock.ctstch.

Import design

In encounter GUI, click design->import design, the following frame comes out, input all needed information like this. Please notice for top cell, you can choose Auto Assign.

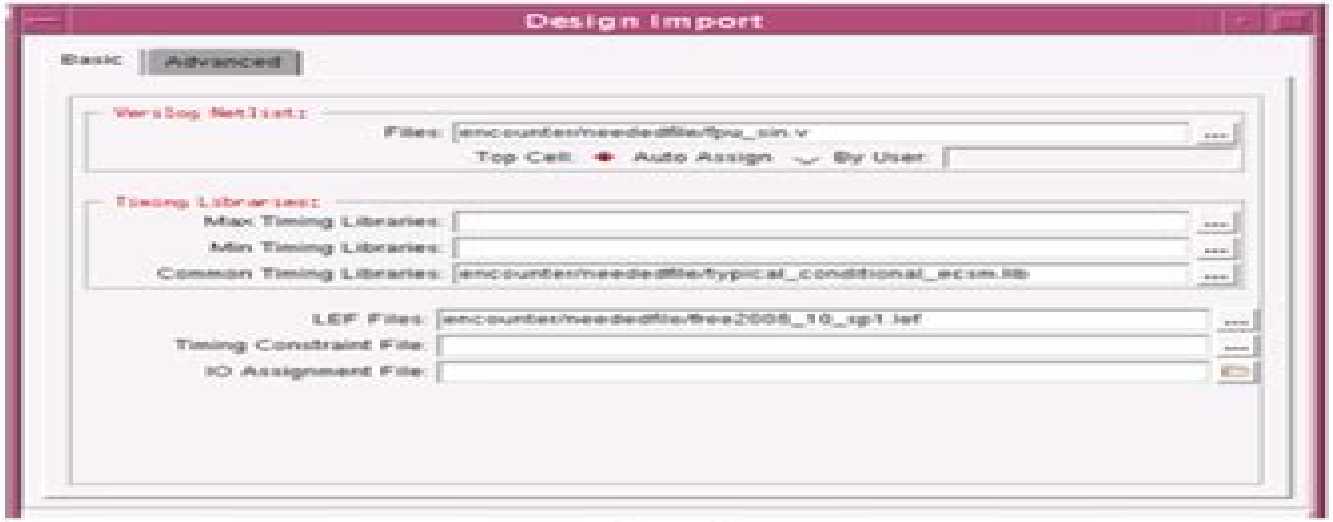

Figure 1

Cadence Encounter User Manual

Mohammad Tehranipoor,Ke Peng,Krishnendu Chakrabarty

Cadence Encounter User Manual:

Testing for Small-Delay Defects in Nanoscale CMOS Integrated Circuits Sandeep K. Goel,Krishnendu Chakrabarty,2017-12-19 Advances in design methods and process technologies have resulted in a continuous increase in the complexity of integrated circuits ICs However the increased complexity and nanometer size features of modern ICs make them susceptible to manufacturing defects as well as performance and quality issues Testing for Small Delay Defects in Nanoscale CMOS Integrated Circuits covers common problems in areas such as process variations power supply noise crosstalk resistive opens bridges and design for manufacturing DfM related rule violations The book also addresses testing for small delay defects SDDs which can cause immediate timing failures on both critical and non critical paths in the circuit Overviews semiconductor industry test challenges and the need for SDD testing including basic concepts and introductory material Describes algorithmic solutions incorporated in commercial tools from Mentor Graphics Reviews SDD testing based on alternative methods that explores new metrics top off ATPG and circuit topology based solutions Highlights the advantages and disadvantages of a diverse set of metrics and identifies scope for improvement Written from the triple viewpoint of university researchers EDA tool developers and chip designers and tool users this book is the first of its kind to address all aspects of SDD testing from such a diverse perspective The book is designed as a one stop reference for current industrial practices research challenges in the domain of SDD testing and recent developments in SDD solutions

Nanometer Technology Designs Nisar Ahmed,2010-02-26 Adopting new fabrication technologies not only provides higher integration and enhances performance but also increases the types of manufacturing defects With design size in millions of gates and working frequency in GHz timing related defects havv become a high proportion of the total chip defects For nanometer technology designs the stuck at fault test alone cannot ensure a high quality level of chips At speed tests using the transition fault model has become a requirement in technologies below 180nm Traditional at speed test methods cannot guarantee high quality test results as they face many new challenges Supply noise including IR drop ground bounce and Ldi dt effects on chip performance high test pattern volume low fault defect coverage small delay defect test pattern generation high cost of test implementation and application and utilizing low cost testers are among these challenges This book discusses these challenges in detail and proposes new techniques and methodologies to improve the overall quality of the transition fault test **Test and Diagnosis for Small-Delay Defects** Mohammad Tehranipoor,Ke Peng,Krishnendu Chakrabarty,2011-09-08 This book will introduce new techniques for detecting and diagnosing small delay defects in integrated circuits Although this sort of timing defect is commonly found in integrated circuits manufactured with nanometer technology this will be the first book to introduce effective and scalable methodologies for screening and diagnosing small delay defects including important parameters such as process variations crosstalk and power supply noise **Design and Process Integration for Microelectronic Manufacturing** ,2005 *Synthesis Methodology for Built-in At-speed Testing*

Yinghua Li,2005 *FPGA ...* ,2006 **The teacher's manual of the tonic sol-fa method** John Curwen,1902 *Electronic Design* ,2007 **EDN** ,2008 **Journal of the United States Infantry Association** ,1950 *Instructions to Young Fencers* Gillan Sheen,1958 **A Low Power Design Methodology with Multi-VDD and Voltage Islands** Huaizhi Wu,2007 CompTIA A+ Certification Study Guide, Seventh Edition (Exam 220-701 & 220-702) Jane Holcombe,Charles Holcombe,2010-05-22 The Best Fully Integrated Study System Available EXAMS 220 701 Operating System Fundamentals Installing Configuring and Upgrading Operating Systems Disk and File Management Troubleshooting and Preventive Maintenance for Windows Using and Supporting Printers Network Basics Installing a Small Office Home Office SOHO Network Troubleshooting Networks Computer Security Fundamentals Implementing and Troubleshooting Security Operational Procedure CD ROM includes Complete Master Exam practice testing engine featuring Two full practice exams Detailed answers with explanations and Score Report performance assessment tool CertCam video training Electronic book for studying on the go With free online registration Two Bonus downloadable MasterExam practice tests Jane Holcombe CompTIA A CompTIA Network MCSE CompTIA CTT has been an independent trainer consultant and course content author since 1984 Charles Holcombe has been an independent trainer and consultant for 30 years and has developed and delivered many training courses He is the coauthor with Jane Holcombe of Survey of Operating Systems Second Edition and several other books The Musical Times and Singing-class Circular ,1912 The Musical Times & Singing-class Circular ,1912 Reference Guide to World Literature Lesley Henderson,Sarah M. Hall,1995 Overviews of writers and works from the ancient Greeks through the 20th century written by subject experts Each author entry provides a detailed overview of the writer s life and works Work entries cover a particular piece of world literature in detail **Conference Proceedings** ,2004 American Organist Thomas Scott Godfrey Burhrman,1922 Consultants & Consulting Organizations Directory Cengage Gale,2009-05-12 **Consultants & Consulting Organizations Directory: Descriptive listings and indexes** ,2009

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