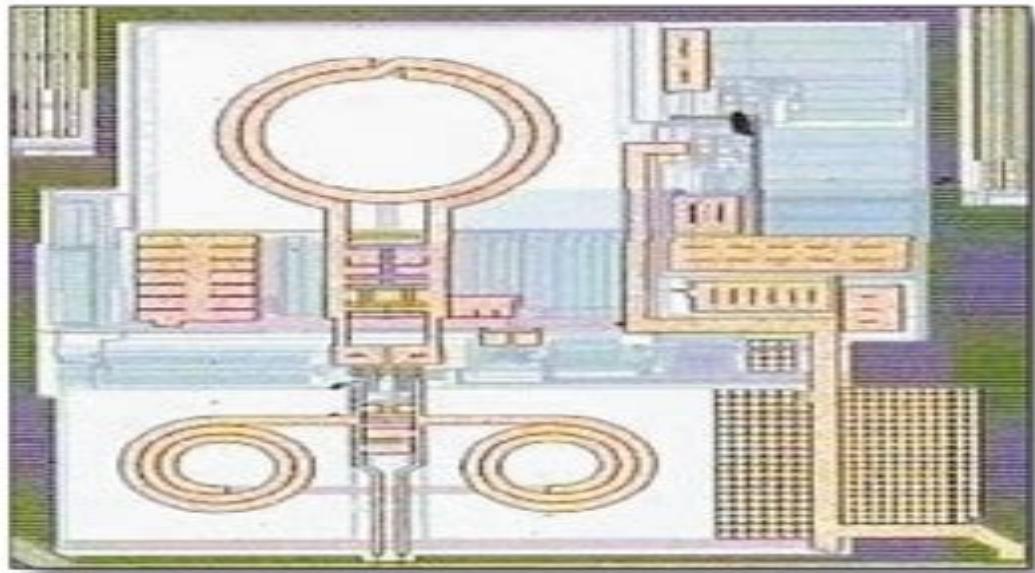


# **CMOS PLLs and VCOs for 4G Wireless**

Adem Aktas  
Mohammed Ismail



Kluwer Academic Publishers

# Cmos Plls And Vcos For 4g Wireless

**Hammad M. Cheema,Reza**

**Mahmoudi,Arthur H.M. van Roermund**

## **Cmos Pls And Vcos For 4g Wireless:**

**CMOS PLLs and VCOs for 4G Wireless** Adem Aktas, Mohammed Ismail, 2007-05-08 CMOS PLLs and VCOs for 4G Wireless is the first book devoted to the subject of CMOS PLL and VCO design for future broadband 4th generation wireless devices. These devices will be handheld centric requiring very low power consumption and small footprint. They will be able to work across multiple bands and multiple standards covering WWAN, GSM, WCDMA, WLAN, 802.11 a/b/g and WPAN, Bluetooth with different modulations, channel bandwidths, phase noise requirements, etc. As such this book discusses design modeling and optimization techniques for low power, fully integrated broadband PLLs and VCOs in deep submicron CMOS. First the PLL and VCO performances are studied in the context of the chosen multi band multi standard radio architecture and the adopted frequency plan. Next a thorough study of the design requirements for broadband PLL/VCO design is conducted together with modeling techniques for noise sources in a PLL and VCO focusing on optimization of integrated phase noise for multi carrier OFDM, 64 QAM type applications. Design examples for multi standard 802.11a/b/g as well as for GSM/WCDMA are fully described and experimental results from 0.18 micron CMOS test chips have demonstrated the validity of the proposed design and optimization techniques. Equally important the work describes techniques for robust high volume production of RF radios in general and for integrated PLL/VCO design in particular including issues such as supply sensitivity, ground bounce and calibration mechanisms. CMOS PLLs and VCOs for 4G Wireless will be of interest to graduate students in electrical and computer engineering, design managers and RFIC designers in wireless semiconductor companies.

**IEEE**

**Circuits & Devices**, 2006    [Nanoelectronic Mixed-Signal System Design](#) Saraju Mohanty, 2015-02-20 Covering both the classical and emerging nanoelectronic technologies being used in mixed signal design this book addresses digital, analog and memory components. Winner of the Association of American Publishers 2016 PROSE Award in the Textbook Physical Sciences/Mathematics category. Nanoelectronic Mixed Signal System Design offers professionals and students a unified perspective on the science, engineering and technology behind nanoelectronics system design. Written by the director of the NanoSystem Design Laboratory at the University of North Texas this comprehensive guide provides a large scale picture of the design and manufacturing aspects of nanoelectronic based systems. It features dual coverage of mixed signal circuit and system design rather than just digital or analog only. Key topics such as process variations, power dissipation and security aspects of electronic system design are discussed. Top down analysis of all stages from design to manufacturing. Coverage of current and developing nanoelectronic technologies not just nano CMOS. Describes the basics of nanoelectronic technology and the structure of popular electronic systems. Reveals the techniques required for design excellence and manufacturability.

**Wireless Technologies** Krzysztof Iniewski, 2017-12-19 Advanced concepts for wireless technologies present a vision of technology that is embedded in our surroundings and practically invisible. From established radio techniques like GSM, 802.11 or Bluetooth to more emerging technologies such as Ultra Wide Band and smart dust motes a common denominator for

future progress is the underlying integrated circuit technology Wireless Technologies responds to the explosive growth of standard cellular radios and radically different wireless applications by presenting new architectural and circuit solutions engineers can use to solve modern design problems This reference addresses state of the art CMOS design in the context of emerging wireless applications including 3G 4G cellular telephony wireless sensor networks and wireless medical application Written by top international experts specializing in both the IC industry and academia this carefully edited work uncovers new design opportunities in body area networks medical implants satellite communications automobile radar detection and wearable electronics The book is divided into three sections wireless system perspectives chip architecture and implementation issues and devices and technologies used to fabricate wireless integrated circuits Contributors address key issues in the development of future silicon based systems such as scale of integration ultra low power dissipation and the integration of heterogeneous circuit design style and processes onto one substrate Wireless sensor network systems are now being applied in critical applications in commerce healthcare and security This reference which contains 25 practical and scientifically rigorous articles provides the knowledge communications engineers need to design innovative methodologies at the circuit and system level

[The British National Bibliography](#) Arthur James Wells,2004    [Advances in Analog and RF IC Design for Wireless Communication Systems](#) Gabriele Manganaro,Domine M W Leenaerts,2013-05-13 Advances in Analog and RF IC Design for Wireless Communication Systems gives technical introductions to the latest and most significant topics in the area of circuit design of analog RF ICs for wireless communication systems emphasizing wireless infrastructure rather than handsets The book ranges from very high performance circuits for complex wireless infrastructure systems to selected highly integrated systems for handsets and mobile devices Coverage includes power amplifiers low noise amplifiers modulators analog to digital converters ADCs and digital to analog converters DACs and even single chip radios This book offers a quick grasp of emerging research topics in RF integrated circuit design and their potential applications with brief introductions to key topics followed by references to specialist papers for further reading All of the chapters compiled by editors well known in their field have been authored by renowned experts in the subject Each includes a complete introduction followed by the relevant most significant and recent results on the topic at hand This book gives researchers in industry and universities a quick grasp of the most important developments in analog and RF integrated circuit design Emerging research topics in RF IC design and its potential application Case studies and practical implementation examples Covers fundamental building blocks of a cellular base station system and satellite infrastructure Insights from the experts on the design and the technology trade offs the challenges and open questions they often face References to specialist papers for further reading    [Design Methodology for RF CMOS Phase Locked Loops](#) Guillermo Bistué,Carlos Quemada,Iñigo Adin,2009 After a review of PLL essentials this uniquely comprehensive workbench guide takes you step by step through operation principles design procedures phase noise analysis layout considerations and CMOS realizations for each PLL

building block You get full details on LC tank oscillators including modeling and optimization techniques followed by design options for CMOS frequency dividers covering flip flop implementation the divider by 2 component and other key factors The book includes design alternatives for phase detectors that feature methods to minimize jitter caused by the dead zone effect You also find a sample design of a fully integrated PLL for WLAN applications that demonstrates every step and detail right down to the circuit schematics and layout diagrams Supported by over 150 diagrams and photos this one stop toolkit helps you produce superior PLL designs faster and deliver more effective solutions for low cost integrated circuits in all RF applications

**Wireless CMOS Frequency Synthesizer Design** J. Craninckx, Michiel Steyaert, 1998-04-30 The recent boom in the mobile telecommunication market has trapped the interest of almost all electronic and communication companies worldwide New applications arise every day more and more countries are covered by digital cellular systems and the competition between the several providers has caused prices to drop rapidly The creation of this essentially new market would not have been possible without the appearance of small low power high performant and certainly low cost mobile terminals The evolution in microelectronics has played a dominant role in this by creating digital signal processing DSP chips with more and more computing power and combining the discrete components of the RF front end on a few ICs This work is situated in this last area i e the study of the full integration of the RF transceiver on a single die Furthermore in order to be compatible with the digital processing technology a standard CMOS process without tuning trimming or post processing steps must be used This should flatten the road towards the ultimate goal the single chip mobile phone The local oscillator LO frequency synthesizer poses some major problems for integration and is the subject of this work The first and also the largest part of this text discusses the design of the Voltage Controlled Oscillator VCO The general phase noise theory of LC oscillators is presented and the concept of effective resistance and capacitance is introduced to characterize and compare the performance of different LC tanks

**60-GHz CMOS Phase-Locked Loops** Hammad M. Cheema, Reza Mahmoudi, Arthur H.M. van Roermund, 2010-06-22 Abstract This chapter lays the foundation for the work presented in latter chapters The potential of 60 GHz frequency bands for high data rate wireless transfer is discussed and promising applications are enlisted Furthermore the challenges related to 60 GHz IC design are presented and the chapter concludes with an outline of the book Keywords Wireless communication 60 GHz Millimeter wave integrated circuit design Phase locked loop CMOS Communication technology has revolutionized our way of living over the last century Since Marconi's transatlantic wireless experiment in 1901 there has been tremendous growth in wireless communication evolving from spark gap telegraphy to today's mobile phones equipped with Internet access and multimedia capabilities The omnipresence of wireless communication can be observed in widespread use of cellular telephony short range communication through wireless local area networks and personal area networks wireless sensors and many others The frequency spectrum from 1 to 6 GHz accommodates the vast majority of current wireless standards and applications Coupled with the availability of low

cost radio frequency RF components and mature integrated circuit IC technologies rapid expansion and implementation of these systems is witnessed. The downside of this expansion is the resulting scarcity of available bandwidth and allowable transmit powers. In addition stringent limitations on spectrum and energy emissions have been enforced by regulatory bodies to avoid interference between different wireless systems. Low Power VCO Design in CMOS Marc Tiebout, 2006-01-25 This work covers the design of CMOS fully integrated low power low phase noise voltage controlled oscillators for telecommunication or datacommunication systems. The need for low power is obvious as mobile wireless telecommunications are battery operated. As wireless telecommunication systems use oscillators in frequency synthesizers for frequency translation the selectivity and signal to noise ratio of receivers and transmitters depend heavily on the low phase noise performance of the implemented oscillators. Datacommunication systems need low jitter the time domain equivalent of low phase noise clocks for data detection and recovery. The power consumption is less critical. The need for multi band and multi mode systems pushes the high integration of telecommunication systems. This is offered by sub micron CMOS featuring digital flexibility. The recent crisis in telecommunication clearly shows that mobile hand sets became mass market high volume consumer products where low cost is of prime importance. This need for low cost products liven research towards CMOS alternatives for the bipolar or BiCMOS solutions in use today.

Design of CMOS Phase-Locked Loops Behzad Razavi, 2020-01-30 This modern pedagogic textbook from leading author Behzad Razavi provides a comprehensive and rigorous introduction to CMOS PLL design featuring intuitive presentation of theoretical concepts extensive circuit simulations over 200 worked examples and 250 end of chapter problems. The perfect text for senior undergraduate and graduate students.

A Comparative Study of Low Phase Noise Voltage-controlled Oscillators (VCOs) in CMOS Technology Hu Jing Yao, 2006 Voltage controlled oscillators VCOs are key components in frequency synthesizers for Radio Frequency RF wireless communications. The design of monolithic VCOs with standard CMOS processes has been the object of several recent research projects. The common goal of these attempts has been to investigate the possibility of meeting the very demanding VCO phase noise specifications without making use of bipolar processes or external components. Two categories of VCOs are studied in this thesis one involving an inductor and the other is inductor free which is a ring oscillator. The study of the phase noise performance of complementary LC VCO shows that most of the phase noises come from the tail current. A modification has been made based on this topology where the tail transistor is removed. However this brings another problem higher power consumption. To overcome this problem sub threshold techniques have been used leading to sub threshold LC VCO. A Ring oscillator is designed at the end because of its wide tuning range and ease of implementation. Schematic simulations layout and post layout simulations are accomplished using TSMC 0.18 um CMOS technology. The performances of the three types of VCOs are compared regarding the oscillating frequency phase noise and tuning range. All of these can be used in the Bluetooth applications. In addition the figure of merit FOM of the designed VCOs is compared with work by other

researchers *60-GHz CMOS Phase-Locked Loops* Hammad M. Cheema, Reza Mahmudi, Arthur van Roermund, 2011-07-16  
Abstract This chapter lays the foundation for the work presented in latter chapters. The potential of 60 GHz frequency bands for high data rate wireless transfer is discussed and promising applications are enlisted. Furthermore the challenges related to 60 GHz IC design are presented and the chapter concludes with an outline of the book. **Keywords** Wireless communication 60 GHz Millimeter wave integrated circuit design Phase locked loop CMOS Communication technology has revolutionized our way of living over the last century. Since Marconi's transatlantic wireless experiment in 1901 there has been tremendous growth in wireless communication evolving from spark gap telegraphy to today's mobile phones equipped with Internet access and multimedia capabilities. The omnipresence of wireless communication can be observed in widespread use of cellular telephony short range communication through wireless local area networks and personal area networks wireless sensors and many others. The frequency spectrum from 1 to 6 GHz accommodates the vast majority of current wireless standards and applications. Coupled with the availability of low cost radio frequency RF components and mature integrated circuit IC technologies rapid expansion and implementation of these systems is witnessed. The downside of this expansion is the resulting scarcity of available bandwidth and allowable transmit powers. In addition stringent limitations on spectrum and energy emissions have been enforced by regulatory bodies to avoid interference between different wireless systems.

**Design and Modeling of Millimeter-wave CMOS Circuits for Wireless Transceivers** Ivan Chee-Hong Lai, Minoru Fujishima, 2008-03-25 Design and Modeling of Millimeter wave CMOS Circuits for Wireless Transceivers describes in detail some of the interesting developments in CMOS millimetre wave circuit design. This includes the re emergence of the slow wave technique used on passive devices the license free 60GHz band circuit blocks and a 76GHz voltage controlled oscillator suitable for vehicular radar applications. All circuit solutions described are suitable for digital CMOS technology. Digital CMOS technology developments driven by Moore's law make it an inevitable solution for low cost and high volume products in the marketplace. Explosion of the consumer wireless applications further makes this subject a hot topic of the day. The book begins with a brief history of millimetre wave research and how the silicon transistor is born. Originally meant for different purposes the two technologies converged and found its way into advanced chip designs. The second part of the book describes the most important passive devices used in millimetre wave CMOS circuits. Part three uses these passive devices and builds circuit blocks for the wireless transceiver. The book completes with a comprehensive list of references for further readings. *Design and Modeling of Millimeter wave CMOS Circuits for Wireless Transceivers* is useful to show the analogue IC designer the issues involved in making the leap to millimetre wave circuit designs. The graduate student and researcher can also use it as a starting point to understand the subject or proceed to innovative from the works described herein. [Design of CMOS Integrated Frequency Synthesizers for Ultra-wideband Wireless Communications Systems](#) Haitao Tong, 2010 Ultra wide band UWB system is a breakthrough in wireless communication as it provides data rate one order higher than existing

ones This dissertation focuses on the design of CMOS integrated frequency synthesizer and its building blocks used in UWB system A mixer based frequency synthesizer architecture is proposed to satisfy the agile frequency hopping requirement which is no more than 9.5 ns three orders faster than conventional phase locked loop PLL based synthesizers Harmonic cancellation technique is extended and applied to suppress the undesired harmonic mixing components Simulation shows that sidebands at 2.4 GHz and 5 GHz are below 36 dBc from carrier The frequency synthesizer contains a novel quadrature VCO based on the capacitive source degeneration structure The QVCO tackles the jeopardous ambiguity of the oscillation frequency in conventional QVCOS Measurement shows that the 5 GHz CSD QVCO in 0.18 m CMOS technology draws 5.2 mA current from a 1.2 V power supply Its phase noise is 120 dBc at 3 MHz o 0set Compared with existing phase shift LC QVCOS the proposed CSD QVCO presents better phase noise and power efficiency Finally a novel injection locking frequency divider ILFD is presented Implemented with three stages in 0.18 m CMOS technology the ILFD draws 3 mA current from a 1.8 V power supply It achieves multiple large division ratios as 6, 12 and 18 with all locking ranges greater than 1.7 GHz and injection frequency up to 11 GHz Compared with other published ILFDs the proposed ILFD achieves the largest division ratio with satisfactory locking range

CMOS VCOs for 1.8GHz and 2.4GHz Bands and Frequency Synthesizer for the IEEE 802.15.4 Standard Sravanthi Kanaparthi,2003

#### **Design of a CMOS VCO and Frequency Divider for 5 GHz**

**Applications** Prithvi Shylendra,2006 This thesis presents the design of a new CMOS Voltage Controlled Oscillator and a frequency divider both of which form important blocks in the design of a PLL synthesizer These components are important because they operate at the highest frequencies within the PLL and also consume most of the power as compared to the other components Both these circuits have been an active topic of research in recent years especially with the scaling of technology bringing hopes of complete system on chip SOC integration at RF frequencies The circuits in this thesis are designed for 5 GHz applications mainly for the IEEE Wireless Local Area Network WLAN 802.11a standard which spans the frequency range from 5.14 GHz to 5.72 GHz The first part of the thesis is an introduction to receiver architectures VCOs and frequency dividers in general The second part deals with the design analysis and simulation results of a novel VCO presented in this work The VCO achieves a tuning range of 130 MHz around a center frequency of 5.70 GHz and a low phase noise of 114 dBc Hz at an offset of 1 MHz The third part presents the design approach adopted here to designing a high frequency divider using dynamic logic and its simulation results The logic used here is True Single Phase Clocking TSPC which makes use of a single clock thereby avoiding the problems of clock skew and loading Two main blocks have been presented the divide by 2 and divide by 2.3 These blocks are then cascaded to achieve higher division ratios

Millimeter Wave CMOS VCO and PLL Design and Phase Noise Mitigation Techniques Zongru Liu,2008

#### **CMOS RF and mm-Wave Transceivers and Synthesizers**

**and Synthesizers** Bharatha Kumar Thangarasu,Nagarajan Mahalingam,Kaixue Ma,Kiat Seng Yeo,2025-10-14 Power consumption has become a critical concern in RF mm wave integrated circuit IC design thanks to new applications from 5G

mobile computing artificial intelligence and the Internet of Things. However big challenges lie ahead for chip designers when they choose to develop ICs using silicon technology for low power and high data rate applications. This is because silicon technology suffers from undesirable energy dissipation due to its lossy substrate and high resistive wiring loss at GHz frequencies. Nonetheless silicon remains the most suitable material satisfying the demands of a rapidly growing semiconductor market through low fabrication cost and ease of achieving system on chip or system in package integration. While long being neglected low power RF mm wave design has vaulted to the forefront of attention in recent years due to the demand for ultra low power transceivers to achieve sustainability. Designing genuinely ubiquitous transceivers for these new applications requires innovations in both system architecture and circuit implementation. This book closes the gap between a typical textbook with theories that are difficult to understand and a design oriented book that offers little insight into actual theories. It evaluates and discusses different circuit topologies receiver and transmitter architectures phase locked loop performance metrics phase noise analysis and sub system level designs that have yet to be reported in other books.

**CMOS Transceiver Design for Short Range Wireless Telemetry** Jonghae Kim, 2001

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