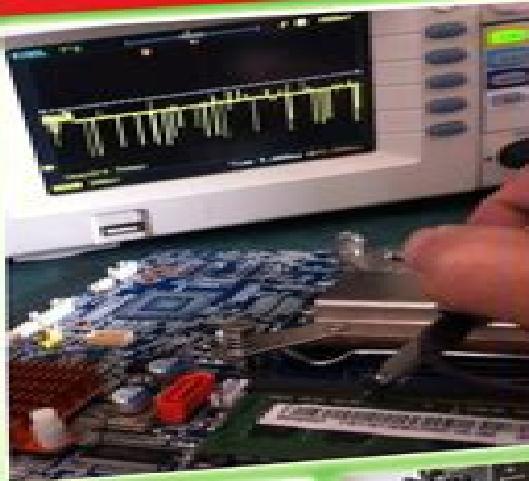


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Optimization and Tuning Techniques for IBM Power Systems Processors Including IBM POWER8 Brian Hall, Peter Bergner, Alon Shalev Housfater, Madhusudanan Kandasamy, Tulio Magno, Alex Mericas, Steve Munroe, Mauricio Oliveira, Bill Schmidt, Will Schmidt, Bernard King Smith, Julian Wang, Suresh Warrier, David Wendt, IBM Redbooks, 2017-03-31 This IBM Redbooks publication focuses on gathering the correct technical information and laying out simple guidance for optimizing code performance on IBM POWER8 processor based systems that run the IBM AIX IBM i or Linux operating systems. There is straightforward performance optimization that can be performed with a minimum of effort and without extensive previous experience or in depth knowledge. The POWER8 processor contains many new and important performance features such as support for eight hardware threads in each core and support for transactional memory. The POWER8 processor is a strict superset of the IBM POWER7 TM processor and so all of the performance features of the POWER7 processor such as multiple page sizes also appear in the POWER8 processor. Much of the technical information and guidance for optimizing performance on POWER8 processors that is presented in this guide also applies to POWER7 and earlier processors except where the guide explicitly indicates that a feature is new in the POWER8 processor. This guide strives to focus on optimizations that tend to be positive across a broad set of IBM POWER processor chips and systems. Specific guidance is given for the POWER8 processor however the general guidance is applicable to the IBM POWER7 IBM POWER7 IBM POWER6 IBM POWER5 and even to earlier processors. This guide is directed at personnel who are responsible for performing migration and implementation activities on POWER8 processor based systems. This includes system administrators, system architects, network administrators, information architects and database administrators, DBAs.

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Table of Contents Chip Level Guide

1. Understanding the eBook Chip Level Guide
 - The Rise of Digital Reading Chip Level Guide
 - Advantages of eBooks Over Traditional Books
2. Identifying Chip Level Guide
 - Exploring Different Genres
 - Considering Fiction vs. Non-Fiction
 - Determining Your Reading Goals
3. Choosing the Right eBook Platform
 - Popular eBook Platforms
 - Features to Look for in an Chip Level Guide
 - User-Friendly Interface
4. Exploring eBook Recommendations from Chip Level Guide
 - Personalized Recommendations
 - Chip Level Guide User Reviews and Ratings

- Chip Level Guide and Bestseller Lists
- 5. Accessing Chip Level Guide Free and Paid eBooks
 - Chip Level Guide Public Domain eBooks
 - Chip Level Guide eBook Subscription Services
 - Chip Level Guide Budget-Friendly Options
- 6. Navigating Chip Level Guide eBook Formats
 - ePUB, PDF, MOBI, and More
 - Chip Level Guide Compatibility with Devices
 - Chip Level Guide Enhanced eBook Features
- 7. Enhancing Your Reading Experience
 - Adjustable Fonts and Text Sizes of Chip Level Guide
 - Highlighting and Note-Taking Chip Level Guide
 - Interactive Elements Chip Level Guide
- 8. Staying Engaged with Chip Level Guide
 - Joining Online Reading Communities
 - Participating in Virtual Book Clubs
 - Following Authors and Publishers Chip Level Guide
- 9. Balancing eBooks and Physical Books Chip Level Guide
 - Benefits of a Digital Library
 - Creating a Diverse Reading Collection Chip Level Guide
- 10. Overcoming Reading Challenges
 - Dealing with Digital Eye Strain
 - Minimizing Distractions
 - Managing Screen Time
- 11. Cultivating a Reading Routine Chip Level Guide
 - Setting Reading Goals Chip Level Guide
 - Carving Out Dedicated Reading Time
- 12. Sourcing Reliable Information of Chip Level Guide
 - Fact-Checking eBook Content of Chip Level Guide
 - Distinguishing Credible Sources

- 13. Promoting Lifelong Learning
 - Utilizing eBooks for Skill Development
 - Exploring Educational eBooks
- 14. Embracing eBook Trends
 - Integration of Multimedia Elements
 - Interactive and Gamified eBooks

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