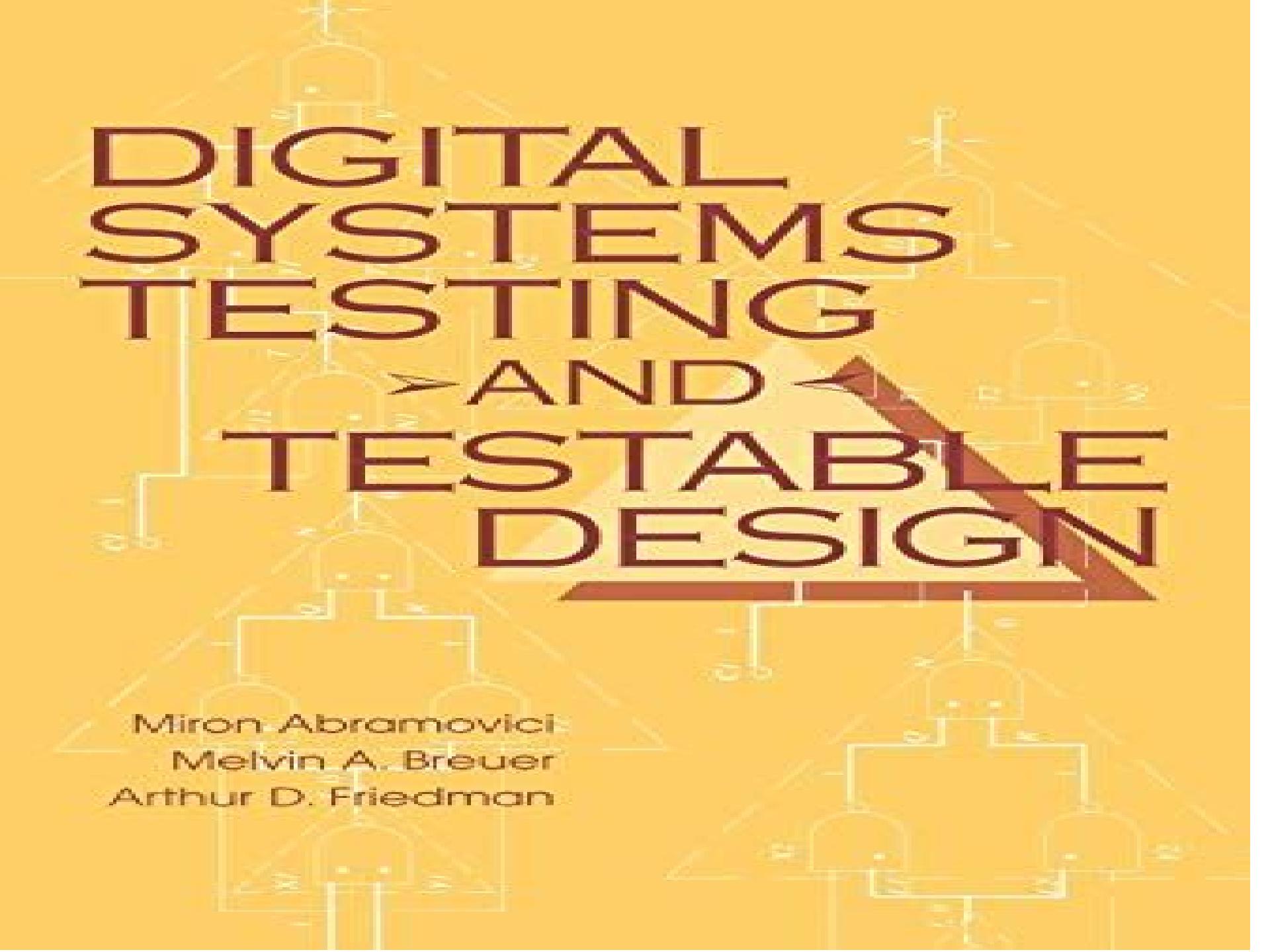


# DIGITAL SYSTEMS TESTING AND TESTABLE DESIGN



Miron Abramovici  
Melvin A. Breuer  
Arthur D. Friedman

# Digital Systems Testing Testable Design

**Ming-Bo Lin**

## Digital Systems Testing Testable Design:

**Digital System Test and Testable Design** Zainalabedin Navabi,2010-12-10 This book is about digital system testing and testable design The concepts of testing and testability are treated together with digital design practices and methodologies The book uses Verilog models and testbenches for implementing and explaining fault simulation and test generation algorithms Extensive use of Verilog and Verilog PLI for test applications is what distinguishes this book from other test and testability books Verilog eliminates ambiguities in test algorithms and BIST and DFT hardware architectures and it clearly describes the architecture of the testability hardware and its test sessions Describing many of the on chip decompression algorithms in Verilog helps to evaluate these algorithms in terms of hardware overhead and timing and thus feasibility of using them for System on Chip designs Extensive use of testbenches and testbench development techniques is another unique feature of this book Using PLI in developing testbenches and virtual testers provides a powerful programming tool interfaced with hardware described in Verilog This mixed hardware software environment facilitates description of complex test programs and test strategies     *Digital Systems Testing and Testable Design* Miron Abramovici,Melvin A. Breuer,Arthur D. Friedman,1994-09-27

This updated printing of the leading text and reference in digital systems testing and testable design provides comprehensive state of the art coverage of the field Included are extensive discussions of test generation fault modeling for classic and new technologies simulation fault simulation design for testability built in self test and diagnosis Complete with numerous problems this book is a must have for test engineers ASIC and system designers and CAD developers and advanced engineering students will find this book an invaluable tool to keep current with recent changes in the field     *Digital Systems Testing & Testable Design* Miron Abramovici,Melvin A. Breuer & Arthur D. Friedman,2001-01-01 This Textbook Provides A Comprehensive And Detailed Treatment Of Digital Systems Testing And Testable Design It Covers Thoroughly Both The Fundamental Concepts And The Latest Advances In This Rapidly Changing Field And Presents Only Theoretical Material That Supports Practical Applications Successfully Used Worldwide This Book Is An Invaluable Tool For Test Engineers Asic And System Designers And Cad Developers

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Electronic Systems provides design engineers with the much needed knowledge base Divided into five major parts this highly useful reference relates design and tests to the development of reliable electronic products shows the main vehicles for design verification examines designs that facilitate testing and investigates how testing is applied to random logic memories FPGAs and microprocessors Finally the last part offers coverage of advanced test solutions for today's very deep submicron designs The authors take a phenomenological approach to the subject matter while providing readers with plenty of opportunities to explore the foundation in detail Special features include An explanation of where a test belongs in the design flow Detailed discussion of scan path and ordering of scan chains BIST solutions for embedded logic and memory blocks Test methodologies for FPGAs A chapter on testing system on a chip Numerous references System-on-Chip Test Architectures Laung-Terng Wang,Charles E. Stroud,Nur A. Touba,2010-07-28 Modern electronics testing has a legacy of more than 40 years The introduction of new technologies especially nanometer technologies with 90nm or smaller geometry has allowed the semiconductor industry to keep pace with the increased performance capacity demands from consumers As a result semiconductor test costs have been growing steadily and typically amount to 40% of today's overall product cost This book is a comprehensive guide to new VLSI Testing and Design for Testability techniques that will allow students researchers DFT practitioners and VLSI designers to master quickly System on Chip Test architectures for test debug and diagnosis of digital memory and analog mixed signal designs Emphasizes VLSI Test principles and Design for Testability architectures with numerous illustrations examples Most up to date coverage available including Fault Tolerance Low Power Testing Defect and Error Tolerance Network on Chip NOC Testing Software Based Self Testing FPGA Testing MEMS Testing and System In Package SIP Testing which are not yet available in any testing book Covers the entire spectrum of VLSI testing and DFT architectures from digital and analog to memory circuits and fault diagnosis and self repair from digital to memory circuits Discusses future nanotechnology test trends and challenges facing the nanometer design era promising nanotechnology test techniques including Quantum Dots Cellular Automata Carbon Nanotubes and Hybrid Semiconductor Nanowire Molecular Computing Practical problems at the end of each chapter for students **The Electronic Design Automation Handbook** Dirk Jansen,2010-02-23 When I attended college we studied vacuum tubes in our junior year At that time an average radio had 5 vacuum tubes and better ones even seven Then transistors appeared in 1960s A good radio was judged to be one with more than ten transistors Later good radios had 15-20 transistors and after that everyone stopped counting transistors Today modern processors running personal computers have over 10 million transistors and more millions will be added every year The difference between 20 and 20M is in complexity methodology and business models Designs with 20 transistors are easily generated by design engineers without any tools whilst designs with 20M transistors can not be done by humans in reasonable time without the help of Prof Dr Gajski demonstrates the Y chart automation This difference in complexity introduced a paradigm shift which required sophisticated methods and tools and introduced design automation into design

practice By the decomposition of the design process into many tasks and abstraction levels the methodology of designing chips or systems has also evolved Similarly the business model has changed from vertical integration in which one company did all the tasks from product specification to manufacturing to globally distributed client server production in which most of the design and manufacturing tasks are outsourced *On-Line Testing for VLSI* Michael Nicolaidis, Yervant Zorian, Dhiraj K. Pradhan, 1998-04-30 Test functions fault detection diagnosis error correction repair etc that are applied concurrently while the system continues its intended function are defined as on line testing In its expanded scope on line testing includes the design of concurrent error checking subsystems that can be themselves self checking fail safe systems that continue to function correctly even after an error occurs reliability monitoring and self test and fault tolerant designs On Line Testing for VLSI contains a selected set of articles that discuss many of the modern aspects of on line testing as faced today The contributions are largely derived from recent IEEE International On Line Testing Workshops Guest editors Michael Nicolaidis Yervant Zorian and Dhiraj Pradhan organized the articles into six chapters In the first chapter the editors introduce a large number of approaches with an expanded bibliography in which some references date back to the sixties On Line Testing for VLSI is an edited volume of original research comprising invited contributions by leading researchers **Introduction to VLSI Systems** Ming-Bo Lin, 2011-11-28 With the advance of semiconductors and ubiquitous computing the use of system on a chip SoC has become an essential technique to reduce product cost With this progress and continuous reduction of feature sizes and the development of very large scale integration VLSI circuits addressing the harder problems requires fundamental understanding **Asian Test Symposium**, 2004 Journal of Information Science and Engineering, 2000 IEEE Circuits & Devices, 2001 **High Level Test Methodology for Crosstalk Faults in Sequential Circuits** Marong Phadoongsidhi, 2004 **IEEE VLSI Test Symposium**, 2005 **Automotive Electronics (Autotech '97)** PEP (Professional Engineering Publishers), Institution of Mechanical Engineers (Great Britain). Automobile Division, 1997 Broad themes of this text on the subject of automotive electronics include EMC and component design software and controllers electronic systems testing and maintenance and power devices *Selected Reprints on Logic Design for Testability* Constantin C. Timoc, 1984 **Proceedings**, 1994 **Digest of Technical Papers**, 1999 Test Response Compaction for Built-in Self Testing Krishnendu Chakrabarty, 1995 Conference Record, Autotestcon '95, August 8-10, 1995 Institute of Electrical and Electronics Engineers, 1995

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