



## The Essentials of Computer Organization and Architecture

Linda Null and Julia Lobur  
Jones and Bartlett Publishers, 2003

# Chapter 5 Instructor's Manual

## Chapter Objectives

Chapter 5, A Closer Look at Instruction Set Architectures, provides a closer look at instruction set architectures, including instruction formats, instruction types, endianness, and addressing modes. Instruction-level pipelining is introduced as well. Real-world ISAs (including Intel, MIPS, and Java) are discussed to reinforce the concepts presented in the chapter.

This chapter should be covered after Chapter 4.

Lectures should focus on the following points:

- **Instruction formats.** Important issues here include instruction length, little versus big endian, register usage (and the use of stacks), and expanding opcodes.
- **Addressing.** Although addressing is an instruction design issue, there are many aspects to consider, the most important of which is addressing modes.
- **Instruction-level pipelining.** The fetch-decode-execute cycle can be overlapped, resulting in faster execution time. Resource conflicts, conditional branching, and data dependencies can slow this process down.
- **Real-world examples of ISAs.** Intel, MIPS, and the Java virtual machine are all presented to reinforce the concepts of the chapter.

## Required Lecture Time

The important concepts in Chapter 5 can typically be covered in 3 lecture hours. However, if a teacher wants the students to have a mastery of all topics in Chapter 5, 8 lecture hours are more reasonable. If lecture time is limited, we suggest that the focus be on instruction formats (including big versus little endian, use of registers, and instruction length) and addressing (with considerable attention paid to the various modes).

# Computer Organization And Architecture Instructor Manual

**Tod Amon, George B. Adams, Edward G. Okie**

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